Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) An asynchronous FIFO circuit comprising:

a memory;

asynchronous reading and writing means of reading a predetermined amount of data from and of writing the predetermined amount of data into said memory on a first-in-first-out basis, the predetermined amount of data including a plurality of words stored in a respective plurality of address locations of the memory;

an error write counter of counting counts up by 1 for each word of the plurality of words containing an error flag that is written into said respective plurality of address locations;

an error read counter of counting up by 1 for each word of the plurality of words containing an error flag that is read from said respective plurality of address locations;

comparing means of comparing a value of said error write counter with a value of said error read counter, said comparing means outputting a logic level of 0 when the value of said error write counter is coincident with the value of said error read counter, and said comparing means outputting a logic level of 1 if the former value is different from the latter value, wherein the logic level of 1 indicates at least one error flag is set in the plurality of words stored in the respective plurality of address locations.

2. (Currently Amended) An asynchronous FIFO circuit comprising:

a memory having addresses for 2^N words, N being a positive integer;

OK to enter SMS 7/26/04